WHAT IS CLAIMED IS:

1. A system that executes code while processing data operations using a non-volatile memory device, comprising:

CPU/Bus/Controller for controlling said memory device;

non volatile array for holding code and data of said system;

non volatile device circuitry for controlling content and activity of said non volatile array; and

logic circuit for enabling automatic suspending and/or automatic resuming of operations.

2. The system of claim 1, wherein said suspending and/or resuming of operations are initiated by a hardware means.

3. The system of claim 1, wherein said non-volatile memory device is a flash memory device.

4. The system of claim 1, wherein said logic circuit enables code execution and data storage/processing facilities within a single chip device with a single silicon die.

5. The system of claim 1, wherein said logic circuit enables code execution and data storage/processing facilities within a bank of single memory chips with single silicon dies.

6. The system of claim 1, wherein said logic circuit is embedded into the memory chip.

7. The system of claim 1, wherein said logic circuit functions from outside the memory chip.

8. The system of claim 1, wherein a pluralism of said logic circuits are embedded into a memory chip.

9. The system of claim 1, wherein a pluralism of said logic circuits function outside a memory chip.

10. The system of claim 1, wherein said logic circuit is operative to monitor status of current operations in said memory chip.

11. The system of claim 1, wherein said logic circuit is operative to mark current status of chip operation so as to make it readable by the OS/application/file management software.

12. The system of claim 1, wherein said CPU/Bus/Controller causes said memory chip to suspend and/or resume operations by signaling to said memory chip to delay CPU /Bus/Controller read operation.

13. A method for executing code while processing data on a non-volatile memory device, comprising the steps of:

i. adding at least one logic circuit to operate with the non-volatile memory device.

ii. monitoring status of current operations in said memory chip.

iii signaling to the CPU/Bus if the chip is available for code execution.

iv. monitoring CPU/Bus activity

v. commanding chip to suspend and/or resume chip operations.

14. A method for executing code while processing data on a non-volatile memory device, comprising the following steps:

i. adding at least one logic circuit to work with the a non-volatile memory chip.

ii. sensing read requests while chip is in program/erase mode/operation.

iii. automatic entering of program and/or erase operations into suspend mode.

iv. signaling to CPU/Bus to wait before executing further read/fetch commands.

v. turning off signal to allow CPU/Bus to (automatically) continue with read/fetch commands

vi. entering of said chip into resume operation to continue program/erase operation.

15. The method of claim 15, wherein said entering into suspend mode includes marking status for reading by OS/application/file management software in the chip.

16. A single flash memory device comprising:

a suspend logic circuit for enabling hardware initiated suspending of data processing

operations; and

a resume logic circuit for enabling hardware initiated resuming of data processing operations.

add A1

add B1